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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,197	03/01/2002	Sanjiv Garg	097749182047.0170009	1234

7590 11/25/2003

STERNE, KESSLER GOLDSTEIN & FOX
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DONAGHUE, LARRY D	

ART UNIT	PAPER NUMBER
2154	8

DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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10/086,197	03/01/2002	Sanjiv Garg	097749182047.0170009	1234

22887 7590 08/28/2003

DISCOVISION ASSOCIATES
INTELLECTUAL PROPERTY DEVELOPMENT
2355 MAIN STREET, SUITE 200
IRVINE, CA 92614

EXAMINER
DONAGHUE, LARRY D

ART UNIT	PAPER NUMBER
2154	8

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PPE

Office Action Summary	Application No.	Applicant(s)	
	Examiner	Group Art Unit	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on Paper No. 5-7.

☑ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 2-20 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 2-20 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

1. Claims 2-20 are presented for examination.

2. Claim 1 has been canceled at the request of applicant.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 2-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of U.S. Patent No. 5,737,624. Although the conflicting claims are not identical, they are not patentably distinct from each other because The claims of 5,737,624 set forth a system which is an obvious variation of claim 2 of the instant application system for register renaming in a computer system capable of out-of-order instruction

execution (claim 1, lines 1-2), comprising: a temporary buffer comprising a plurality of storage locations for storing execution results (claim 13, lines 2-4), wherein an execution result for an instruction in an instruction window is stored in one of said plurality of storage locations (claim 13, lines 2-4), said one of said plurality of storage locations being assigned to said instruction in said instruction window(claim 13, lines 2-7); and tag assignment logic that outputs a tag comprising a temporary buffer storage location address in place of a register address for an operand of a first instruction claim 13, lines 5-13), wherein said temporary buffer storage location address is an address of said operand in one of said plurality of storage locations if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window for said operand (claim 13, lines 8-13).

5. Garg et al. was cited by examiner on paper no. 4.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 2-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (5,448,705).

Nguyen et al. was cited by examiner on paper no. 4.

8. Nguyen taught the invention (claim 13) as claimed including a computer system (100), comprising: a memory unit for storing program instructions (132, 110, 112); a bus coupled to said memory unit for retrieving said program instructions (114, 136) ; and a processor (104) coupled to said bus, wherein said processor comprises a register renaming system (496), comprising: a temporary buffer comprising a plurality of storage locations for storing execution results (552), wherein an execution result for an instruction in an instruction window is stored in one of said plurality of storage locations, said one of said plurality of storage locations being assigned to said instruction in said instruction window; and tag assignment logic that outputs a tag comprising a temporary buffer storage location address in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window for said operand, wherein said temporary buffer storage location address is an address of said operand in one of said plurality of storage locations (col. 37, line 1 - col. 38, line 12).

9. As to claim 9, Nguyen et al. taught said processor further comprises termination logic that transfers said execution results in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions in said instruction window (col. 37, lines 53-63).

10. As to claim 10, Nguyen et al. taught said termination logic transfers a plurality of execution results from said temporary buffer to said register file simultaneously (col. 37, lines 53-63).

11. As to claim 11, Nguyen et al. taught said termination logic transfers an execution result for an instruction from said temporary buffer to said register file when all execution results for all prior instructions are retireable (col. 37, lines 53-63).

12. As to claim 12, Nguyen et al. taught said tag further comprises an identifier that indicates whether said address within said tag is an address within a register file or said plurality of storage locations (col.36, lines 58-68).

13. As to claim 13, Nguyen et al. taught said processor further comprises register file port multiplexers that pass said tag to read address ports of said temporary buffer for accessing said execution results (col. 36, lines 35-63).

As to claims 2-12 and 14-20 fail to teach above or beyond claims 8-13, and is reject for the reason set forth, above.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

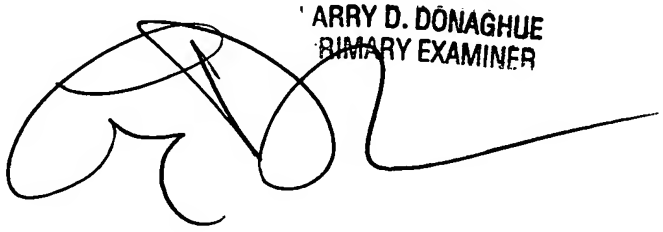
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to L. Donaghue whose telephone number is (703) 305-9675. The examiner can normally be reached on M-F from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An , can be reached on (703) 305-9678. The fax phone number for an official fax is (703) 746-7238, an after-final fax is 703-746-7238 and a draft or non-official fax is 703-746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.



FORM PTO-1449	ATTY. DOCKET NO. 2047.0170009 (As Corrected)	APPLICATION NO. 10/086,197
INFORMATION DISCLOSURE STATEMENT	APPLICANT GARG *et al.*	
	FILING DATE March 1, 2002	GROUP 2154

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	4,626,989	12/1986	Torii			
	AB1	4,675,806	06/1987	Uchida			
	AC1	4,722,049	01/1988	Lahti			
	AD1	4,807,115	02/1989	Torng			
	AE1	4,901,233	02/1990	Liptay			
	AF1	4,903,196	02/1990	Pomerene *et al.*			
	AG1	4,942,525	07/1990	Shintani *et al.*			
	AH1	4,992,938	02/1991	Cocke *et al.*			
	AI1	5,067,069	11/1991	Fite *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	O 515 166 A1	11/1992	EP			Yes No
	AK1	0 533 337 A1	03/1993	EP			Yes No
	AL1	WO 91/20031 A1	12/1991	PCT			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	1	Acosta, R. D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, IEEE, Vol. C-35, No. 9, September 1986, pp. 815-828.
	AN	1	Agerwala, T. and Cocke, J., *High Performance Reduced Instruction Set Processors*, IBM Research Division, March 31, 1987, pp. 1-61.
	AO	1	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," *ESOP '88, 2nd European Symposium on Programming*, Springer, ISBN 3-540-19027-9, 1988, pp. 221-235.
	AP	1	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, January 23, 1990, 24 pages.
	AQ	1	Butler, M. *et al.*, "Single Instruction Stream Parallelism Is Greater Than Two," *18th Annual International Symposium on Computer Architecture*, Vol. 19, No. 3, ACM, May 1991, pp. 276-286.

EXAMINER	DATE CONSIDERED
	09/22/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

::ODMA\MHODMA\SKGF_DC1;126875;1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 2047.0170009 (As Corrected)	APPLICATION NO. 10/086,197
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	5,109,495	04/1992	Fite *et al.*			
	AB2	5,142,633	08/1992	Murray *et al.*			
	AC2	5,214,763	05/1993	Blaner *et al.*			
	AD2	5,222,244	06/1993	Carbine *et al.*			
	AE2	5,226,126	07/1993	McFarland *et al.*			
	AF2	5,230,068	07/1993	Van Dyke *et al.*			
	AG2	5,251,306	10/1993	Tran			
	AH2	5,261,071	11/1993	Lyon			
	AI2	5,345,569	09/1994	Tran			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2						Yes No
	AK2						Yes No
	AL2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	2	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, IEEE, Vol. 14, September 1981, pp. 18-27.
	AN	2	Colwell, R.P. *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, IEEE Computer Society, October 1987, pp. 180-192.
	AO	2	Dwyer, H., III, Ph.D., *A Multiple, Out-of-Order, Instruction Issuing System For Superscalar Processors*, Dissertation for Cornell University, UMI Dissertation Services, August 1991, pp. iii-xvi and 1-249.
	AP	2	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Transactions On Computers*, IEEE, December 1972, pp. 1411-1415.
	AQ	2	Gee, J. *et al.*, "The Implementation of Prolog via VAX 8600 Microcode," *International Symposium on Microarchitecture: Proceedings of the 19th Annual Workshop on Microprogramming*, ACM, 1986, pp. 68-74.

EXAMINER	DATE CONSIDERED 08/22/07

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	5,355,457	10/1994	Shebanow *et al.*			
	AB3	5,398,330	03/1995	Johnson			
	AC3	5,442,757	08/1995	McFarland *et al.*			
	AD3	5,448,705	09/1995	Nguyen *et al.*			
	AE3	5,487,156	01/1996	Popescu *et al.*			
	AF3	5,497,499	03/1996	Garg *et al.*			
	AG3	5,561,776	10/1996	Popescu *et al.*			
	AH3	5,574,927	11/1996	Scantlin			
	AI3	5,592,636	01/1997	Popescu *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3						Yes No
	AK3						Yes No
	AL3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	3	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," *Proceedings of the 2nd International Conference on Supercomputing*, ACM, 1988, pp. 442-452.
	AN	3	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, IEEE & ACM, October 5-7, 1982, pp. 114-120.
	AO	3	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," *Proceedings 1989 IEEE International Conference on Computer Design: VLSI in Computers and Processors*, IEEE, October 1989, pp. 134-137.
	AP	3	Horst, R.W. *et al.*, "Multiple Instruction Issue in the NonStop Cyclone Processor," *Proceedings of the 17th Annual International Symposium on Computer Architecture*, ACM, 1990, pp. 216-226.
	AQ	3	Hwu, W. *et al.*, "An HPS Implementation of VAX: Initial Design and Analysis," *Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences*, 1986, pp. 282-291.

EXAMINER	DATE CONSIDERED
	08/22/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	5,625,837	04/1997	Popescu *et al.*			
	AB4	5,627,983	05/1997	Popescu *et al.*			
	AC4	5,708,841	01/1998	Popescu *et al.*			
	AD4	5,737,624	04/1998	Garg *et al.*			
	AE4	5,768,575	06/1998	McFarland *et al.*			
	AF4	5,778,210	07/1998	Henstrom *et al.*			
	AG4	5,797,025	08/1998	Popescu *et al.*			
	AH4	5,832,205	11/1998	Kelly *et al.*			
	AI4	5,832,293	11/1998	Popescu *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4						Yes No
	AK4						Yes No
	AL4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	4	Hwu, W. W. and Patt, Y.N., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," *IEEE Transactions On Computers*, IEEE, Vol. C-36, No. 12, December 1987, pp. 1496-1514.
	AN	4	Hwu, W. and Patt, Y.N., "Design Choices for the HPSm Microprocessor Chip," *Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences*, 1987, pp. 330-336.
	AO	4	Hwu, W.W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual International Symposium on Computer Architecture*, IEEE, June 1988, pp. 45-53.
	AP	4	Hwu, W. and Patt, Y.N., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," *Proceedings of the 13th Annual Symposium on Computer Architecture*, IEEE, 1986, pp. 297-306.
	AQ	4	Hwu, W. and Patt, Y.N., "HPSm2: A Refined Single-chip Microengine," Proceedings of *HICSS-21- Volume I - Architecture*, 1988, pp. 30-40.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5	5,974,526	10/1999	Garg *et al.*			
	AB5	6,289,433 B1	09/2001	Garg *et al.*			
	AC5						
	AD5						
	AE5						
	AF5						
	AG5						
	AH5						
	AI5						

FOREIGN PATENT DOCUMENTS

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	AJ5						Yes No
	AK5						Yes No
	AL5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	5	*IBM Journal of Research and Development*, IBM, Vol. 34, No. 1, January 1990, pp. 1-70.
	AN	5	Johnson, W. M., *Super-Scalar Processor Design*, Dissertation for Stanford University, 1989, pp. ii-xiii and 1-134.
	AO	5	Jouppi, N.P. and Wall, D.W., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings - 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, ACM, April 1989, pp. 272-282.
	AP	5	Jouppi, N.P., "Integration and Packaging Plateaus of Processor Performance," *International Conference of Computer Design*, IEEE, October 2-4, 1989, pp. 229-232.
	AQ	5	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," *IEEE Transactions on Computers*, IEEE, Vol. 38, No. 12, December 1989, pp. 1645-1658.

EXAMINER	DATE CONSIDERED
	08/22/03

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	AA6						
	AB6						
	AC6						
	AD6						
	AE6						
	AF6						
	AG6						
	AH6						
	AI6						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6						Yes No
	AK6						Yes No
	AL6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	6	Keller, R.M., "Look-Ahead Processors," *Computing Surveys*, ACM, Vol. 7, No. 4, December 1975, pp. 177-195.
	AN	6	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," *Annu. Rev. Comput. Sci.*, Annual Reviews, Inc., Vol. 4, 1990, pp. 173-201.
	AO	6	Lightner, B.D. and Hill, G., "The Metaflow Lightning Chip Set," *COMPCON Spring '91 digest of papers*, IEEE Computer Society Press, February 25 - March 1, 1991, pp. 13-18.
	AP	6	Melvin, S. and Patt, Y., "Exploiting Fine-Grained Parallelism Through a Combination of Hardware and Software Techniques," *The 18th Annual International Symposium on Computer Architecture*, Vol. 19, No. 3, ACM, May 1991, pp. 287-296.
	AQ	6	Murakami, K. *et al.*, "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," *Proceedings of the 16th Annual International Symposium on Computer Architecture*, ACM, 1989, pp. 78-85.

EXAMINER	DATE CONSIDERED 8/12/03

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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	AA8						
	AB8						
	AC8						
	AD8						
	AE8						
	AF8						
	AG8						
	AH8						
	AI8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8						Yes No
	AK8						Yes No
	AL8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	8	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching And Their CISC Performance Potential", IEEE, 1991, pp. 263-266.
	AN	8	Pleszkun, A.R. and Sohi, G.S., "The Performance Potential of Multiple Functional Unit Processors*," *Proceedings of the 15th Annual International Symposium on Computer Architecture*, IEEE, June 1988, pp. 37-44.
	AO	8	Pleszkun, A.R. *et al.*, "WISQ: A Restartable Architecture Using Queues," *Proceedings of the 14th International Symposium on Computer Architecture*, ACM, June 1987, pp. 290-299.
	AP	8	Popescu, V. *et al.*, "The Metaflow Architecture", *IEEE Micro*, IEEE, June 1991, pp. 10-13 and 63-73.
	AQ	8	Smith, M.D. *et al.*, "Boosting Beyond Static Scheduling in a Superscalar Processor," *ACM SIGARCH Computer Architecture News*, ACM, Vol. 18, Issue 3, June 1990, pp. 344-354.

EXAMINER	DATE CONSIDERED
	8/12/10

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 2047.0170009 (As Corrected)	APPLICATION NO. 10/086,197
	APPLICANT GARG *et al.*	
	FILING DATE March 1, 2002	GROUP 2154

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7						Yes No
	AK7						Yes No
	AL7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	7	Patt, Y.N. *et al.*, "Critical Issues Regarding HPS, A High Performance Microarchitecture," *Proceedings of the 18th Annual Workshop on Microprogramming*, ACM, December 3-6, 1985, pp. 109-116.
	AN	7	Patt, Y. *et al.*, "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," *COMPCON '86 digest of papers*, 1986, pp. 254-258.
	AO	7	Patt, Y.N. *et al.*, "HPS, A New Microarchitecture: Rationale and Introduction," *Proceedings of the 18th Annual Workshop on Microprogramming*, ACM, December 1985, pp. 103-108.
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	AQ	7	Patterson, D.A. and Hennessy, J.L, *Computer Architecture A Quantitative Approach*, Morgan Kaufmann Publishers, Inc., 1990, pp. xi-xv, 257-278, 290-314 and 449.

EXAMINER	DATE CONSIDERED 8/27/07

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9						Yes No
	AK9						Yes No
	AL9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	9	Smith, J.E. and Pleszkun, A.R.,"Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, IEEE, June 1985, pp. 36-44.
	AN	9	Smith, M.D. *et al.*, "Limits on Multiple Instruction Issue," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, ACM, April 1989, pp. 290-302.
	AO	9	Sohi, G. S. and Vajapeyam, S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," *Proceedings of the 14th Annual International Symposium on Computer Architecture*, ACM, June 2-5, 1987, pp. 27-34.
	AP	9	Swensen, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," *Conference Proceedings: 1988 International Conference on Supercomputing*, ICS, July 4-8, 1988, pp. 346-353.
	AQ	9	Thornton, J.E., *Design of a Computer: The Control Data 6600*, Control Data Corporation, 1970, pp. 58-140.

EXAMINER	DATE CONSIDERED
	08/22/03

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	AA10						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ10						Yes No
	AK10						Yes No
	AL10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	10	Tjaden, G.S. and Flynn, M.J., "Detection and Parallel Execution of Independent Instructions," *IEEE Transactions On Computers*, IEEE, Vol. C-19, No. 10, October 1970, pp. 889-895.
	AN	10	Tjaden, G.S. and Flynn, M.J., "Representation of Concurrency with Ordering Matrices," *IEEE Transactions On Computers*, IEEE, Vol. C-22, No. 8, August 1973, pp. 752-761.
	AO	10	Tjaden, G.J., *Representation and Detection of Concurrency Using Ordering Matrices*, Dissertation for The Johns Hopkins University, UMI Dissertation Services, 1972, pp. 1-199.
	AP	10	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journal of Research and Development*, International Business Machines Corporation, Vol. 11, No. 1, January 1967, pp. 25-33.
	AQ	10	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," *Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, Vol. I, University of Hawaii, 1986, pp. 41-50.

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	AA11						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11						Yes No
	AK11						Yes No
	AL11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	11	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 1, January 1992, pp. 17-28.
	AN	11	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *Symposium on ULSI Circuits Design Digest of Technical Papers*, May 1990, 2 pages.
	AO	11	Wedig, R.G., *Detection of Concurrency In Directly Executed Language Instruction Streams*, Dissertation for Stanford University, UMI Dissertation Services, June 1982, pp. ii, iii, v, vii-xv and 1-179.
	AP	11	Weiss, S. and Smith, J.E., "Instruction Issue Logic in Pipelined Supercomputers," *IEEE Transactions on Computers*, IEEE, Vol. C-33, No. 11, November 1984, pp. 1013-1022 (77-86).
	AQ	11	Wilson, J.E. *et al.*, "On Tuning the Microarchitecture of an HPS Implementation of the VAX," *MICRO 20: Proceedings of the 20th Annual Workshop on Microprogramming*, ACM SIGMICRO and IEEE CS TC-MICRO, December 1-4, 1987, pp. 162-167.

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